CLAIMS

We claim:

1 A memory system having a stub configuration comprising:

a controller for generating a first clock signal, a control signal, an address signal and data signals on a data bus, the data bus, first clock signal, control signal, and address signal being arranged in a stub configuration; and

a memory module including memory devices coupled to the controller, the memory module receiving the first clock signal and the control signal that includes a read or write command;

the memory module, in response to the write command, initiating a write operation for writing the data signals from the data bus to the memory devices in synchronization with the first clock signal; and

the memory module, in response to the read command, initiating a read operation for reading data from the memory devices to the data bus in synchronization with the first clock signal and generating a second clock signal in response to the first clock signal, the second clock signal being provided to the controller, the controller receiving the data signals on the data bus in response to the second clock signal during the read operation.

2 The memory system of claim 1 wherein the first clock signal comprises a write clock and wherein the second clock signal comprises a read clock.

3 The memory system of claim 1 wherein the system comprises multiple memory modules and wherein the multiple memory modules each generate independent second clock signals, the second clock signals each being different in phase.

4 The memory system of claim 3 wherein the phases of the multiple second clock signals are different in phase due to the difference in propagation delay between each of the memory modules and the controller.

5 The memory system of claim 1 wherein the propagation delay of the second clock signal from the memory module to the controller is substantially equal to that of the data bus.

6 The memory system of claim 1 wherein the memory module further includes a control/address buffer that receives the first clock signal and the control signal and generates the second clock signal in response to the first clock signal.

7 The memory system of claim 1 wherein the memory module further includes a phase locked loop that receives the first clock signal and generates the second clock signal in response to the first clock signal.

8 The memory system of claim 1 wherein the memory module further includes a delay locked loop that receives the first clock signal and generates the second clock signal in response to the first clock signal.

9 The memory system of claim 1 wherein the memory module includes a return path that is coupled to a first clock signal line that receives the first clock signal for generating the second clock signal in response to the first clock signal.

10 The memory system of claim 9 wherein the memory module further includes a capacitor having a capacitance that is selected to compensate for capacitive loading on the data bus by the memory device of the memory module; the capacitor being coupled to a junction of the first clock signal line and the return path.

11 The memory system of claim 1 wherein the memory system includes first and second memory modules, the memory module generating respective first and second independent return clock signals as the second clock signal, and further comprising a motherboard coupling the first and second memory modules and the controller, the motherboard including the data bus, a control bus for transfer of the control signal; an address bus for transfer of the address signal; a first clock signal line for transfer of the first clock signal and first and second independent return clock signal lines for transfer of the first and second return clock signals.

12 The memory system of claim 11 wherein the first and second return clock signal lines are crossed on the motherboard between the first and second modules.

13 The memory system of claim 11 wherein the first return clock signal line is coupled to a dummy load on the second memory module and wherein the second return clock signal line is coupled to a dummy load on the first memory module.

14 The memory system of claim 13 wherein the dummy load comprises a load capacitor or a dummy pin.

15 The memory system of claim 13 wherein the dummy load is selected to match the capacitance loading of the data bus.

16 The memory system of claim 1 further comprising a first flag signal generated by the controller, the memory module, in response to the first flag signal, controlling timing of initiation of the write operation or read operation, and if a read operation is commanded, generating a second flag signal in response to the first flag signal, the second flag signal being provided to the controller, the controller receiving the data signals on the data bus in response to the second clock signal and the second flag signal during a read operation.

17 The memory system of claim 16 wherein the memory system includes first and second memory modules, the memory module generating respective first and second independent second flag signals, and further comprising a motherboard coupling the first and second memory modules and the controller, the motherboard including the data bus, a control bus for transfer of the control signal, an address bus for transfer of the address signal; a first flag signal line for transfer of the first flag signal, and first and second independent return flag signal lines for transfer of the first and second return flag signals, the first flag signal line and the first and second return flag signal lines being routed with the control bus and the address bus.

18 The memory system of claim 17 wherein the first and second return flag signal lines are crossed on the motherboard between the first and second modules.

19 The memory system of claim 17 wherein the first return flag signal line is coupled to a dummy load on the second memory module and wherein the second return flag signal line is coupled to a dummy load on the first memory module.

20 The memory system of claim 19 wherein the dummy load comprises a load capacitor or a dummy pin.

21 The memory system of claim 19 wherein the dummy load is selected to match the capacitance loading of the data bus.

22 The memory system of claim 1 further comprising a control buffer mounted to a first side of the memory module, and further comprising a dummy load for coupling to a first signal line of the control buffer to provide load matching with a load experienced by a second signal line of the memory devices mounted to both first and second sides of the memory module.

23 The memory system of claim 22 wherein the dummy load comprises a load capacitor or a dummy pin.

24 The memory system of claim 22 wherein the first signal line comprises the first clock signal or the second clock signal, and wherein the second signal line comprises the data bus or the first clock signal.

25 A memory system having a stub configuration comprising:

a controller for generating a first flag signal, a control signal, an address signal, and data signals on a data bus, the data bus, first flag signal, control signal, and address signal being arranged in a stub configuration; and

a memory module including memory devices coupled to the controller, the memory module receiving the first flag signal and the control signal that includes a read or write command;

the memory module, in response to the write command, initiating a write operation for writing the data signals from the data bus to the memory devices in response to the first flag signal; and

the memory module, in response to the read command, initiating a read operation for reading data from the memory devices to the data bus in response to the first flag signal and generating a second flag signal in response to the first flag signal, the second flag signal being provided to the controller, the controller receiving the data signals on the data bus in response to the second flag signal during the read operation.

26 The memory system of claim 25 further comprising a first clock signal generated by the controller, the memory module, in response to the first clock signal, initiating the write operation or read operation, and if a read operation is commanded, generating a second

clock signal in response to the first clock signal, the second clock signal being provided to the controller, the controller receiving the data signals on the data bus in response to the second clock signal and the second flag signal during a read operation.

27 The memory system of claim 26 wherein the first clock signal comprises a write clock and wherein the second clock signal comprises a read clock.

28 The memory system of claim 26 wherein the system comprises multiple memory modules and wherein the multiple memory modules each generate independent second clock signals, the second clock signals each being different in phase.

29 The memory system of claim 28 wherein the phases of the multiple second clock signals are different in phase due to the difference in propagation delay between each of the memory modules and the controller.

30 The memory system of claim 26 wherein the propagation delay of the second clock signal from the memory module to the controller is substantially equal to that of the data bus.

31 The memory system of claim 26 wherein the memory module further includes a control/address buffer that receives the first clock signal and the control/address signal and generates the second clock signal in response to the first clock signal.

32 The memory system of claim 26 wherein the memory module further includes a phase locked loop that receives the first clock signal and generates the second clock signal in response to the first clock signal.

33 The memory system of claim 26 wherein the memory module further includes a delay locked loop that receives the first clock signal and generates the second clock signal in

response to the first clock signal.

34 The memory system of claim 26 wherein the memory module includes a return path that is coupled to a first clock signal line that receives the first clock signal for generating the second clock signal in response to the first clock signal.

35 The memory system of claim 34 wherein the memory module further includes a capacitor having a capacitance that is selected to compensate for capacitive loading on the data bus by the memory of the memory module; the capacitor being coupled to a junction of the first clock signal line and the return path.

36 The memory system of claim 26 wherein the memory system includes first and second memory modules, the memory module generating respective first and second independent return clock signals as the second clock signal, and further comprising a motherboard coupling the first and second memory modules and the controller, the motherboard including the data bus, a control bus for transfer of the control signal, an address bus for transfer of the address signal, a first clock signal line for transfer of the first clock signal and first and second independent return clock signal lines for transfer of the first and second return clock signals.

37 The memory system of claim 36 wherein the first and second return clock signal lines are crossed on the motherboard between the first and second modules.

38 The memory system of claim 36 wherein the first return clock signal line is coupled to a dummy load on the second memory module and wherein the second return clock signal line is coupled to a dummy load on the first memory module.

39 The memory system of claim 38 wherein the dummy load comprises a load capacitor or a

dummy pin.

40 The memory system of claim 38 wherein the dummy load is selected to match the capacitance loading of the data bus.

41 The memory system of claim 25 wherein the memory system includes first and second memory modules, the memory module generating respective first and second independent second flag signals, and further comprising a motherboard coupling the first and second memory modules and the controller, the motherboard including the data bus, a control bus for transfer of the control signal, an address bus for transfer of the address signal, a first flag signal line for transfer of the first flag signal, and first and second independent return flag signal lines for transfer of the first and second return flag signals, the first flag signal line and the first and second return flag signal lines being routed with the control and address buses.

42 The memory system of claim 41 wherein the first and second return flag signal lines are crossed on the motherboard between the first and second modules.

43 The memory system of claim 41 wherein the first return flag signal line is coupled to a dummy load on the second memory module and wherein the second return flag signal line is coupled to a dummy load on the first memory module.

44 The memory system of claim 43 wherein the dummy load comprises a load capacitor or a dummy pin.

45 The memory system of claim 44 wherein the dummy load is selected to match the capacitance loading of the data bus.

46 The memory system of claim 25 further comprising a control buffer mounted to a first side of the memory module, and further comprising a dummy load for coupling to a first signal line of the control buffer to provide load matching with a load experienced by a second signal line of the memory devices mounted to both first and second sides of the memory module.

47 The memory system of claim 46 wherein the dummy load comprises a load capacitor or a dummy pin.

48 The memory system of claim 46 wherein the first signal line comprises the first flag signal or the second flag signal, and wherein the second signal line comprises the data bus.

49 The memory system of claim 25 wherein the memory module further includes a control buffer that receives the first flag signal and the control signal and generates the second flag signal in response to the first flag signal.

50 The memory system of claim 25 wherein the memory module further includes a phase locked loop that receives the first flag signal and generates the second flag signal in response to the first flag signal.

51 The memory system of claim 25 wherein the memory module further includes a delay locked loop that receives the first flag signal and generates the second flag signal in response to the first flag signal.

52 The memory system of claim 25 wherein the memory module includes a return path that is coupled to a first flag signal line that receives the first flag signal for generating the second flag signal in response to the first flag signal.

53 The memory system of claim 52 wherein the memory module further includes a capacitor having a capacitance that is selected to compensate for capacitive loading on the data bus by the memory device of the memory module; the capacitor being coupled to a junction of the first flag signal line and the return path.

54 A memory system having a stub configuration comprising:

a controller for generating a first clock signal, a control signal, an address signal and data signals on a data bus, the data bus, first clock signal, control signal, and address signal being arranged in a stub configuration;

a second clock signal generator for generating a second clock signal;

a memory module including memory devices coupled to the controller, the memory module receiving the first clock signal, the second clock signal and the control signal that includes a read or write command;

the first clock signal propagating from the controller to the memory module in a first direction of propagation, and the second clock signal propagating from the memory module to the controller in a second direction of propagation;

the memory module, in response to the write command, initiating a write operation for writing the data signals from the data bus to the memory devices in synchronization with the first clock signal; and

the memory module, in response to the read command, initiating a read operation for reading data from the memory to the data bus in response to the second clock signal, the controller receiving the data signals on the data bus in response to the second clock signal during the read operation.

55 The memory system of claim 54 wherein the first clock signal comprises a write clock and wherein the second clock signal comprises a read clock.

56 The memory system of claim 55 wherein the memory controller further compensates for phase difference between the received second clock signal and the data signals on the data bus.

57 A memory system having a stub configuration comprising:

a controller for generating a first clock signal, a control signal, an address signal, and data signals on a data bus, the data bus, first clock signal, control signal, and address signal being arranged in a stub configuration; and

a memory module coupled to the controller, the memory module having first and second faces including memory devices on both first and second faces and including a control and address buffer on the first face, the memory module receiving the first clock signal, the address signal and the control signal that includes a read or write command;

the memory module, in response to the write command, initiating a write operation for writing the data signals from the data bus to the memory devices in synchronization with the first clock signal; and

the memory module, in response to the read command, initiating, at the control and address buffer, a read operation for reading data from the memory devices to the data bus in synchronization with the first clock signal and generating a second clock signal in response to the first clock signal, the second clock signal being provided to the controller, the controller receiving the data signals on the data bus in response to the second clock signal during the read operation.

58 A memory system having a stub configuration comprising:

a controller for generating a first flag signal, a control signal, an address signal, and data signals on a data bus, the data bus, first flag signal, control signal, and address signal being arranged in a stub configuration;

a memory module including memory devices coupled to the controller, the memory module receiving the first flag signal and the control signal that includes a read or write command;

the memory module, in response to the write command, initiating a write operation for writing the data signals from the data bus to the memory devices in response to the first flag signal; and

the memory module, in response to the read command, initiating a read operation for reading data from the memory devices to the data bus in response to the first flag signal and generating a second flag signal in response to the first flag signal, the second flag signal being provided to the controller, the controller receiving the data signals on the data bus in response to the second flag signal during the read operation; and

a motherboard coupling the memory module and the controller, the motherboard including the data bus, a control bus for transfer of the control signal, an address bus for transfer of the address signal, a first flag signal line for transfer of the first flag signal, and a second flag signal line for transfer of the second flag signal, the first flag signal line and the second flag signal line being routed with the control and address buses.

59 The memory system of claim 58 wherein the memory module comprises first and second memory modules, and wherein the first and second memory modules generate independent first and second return flag signals respectively as the second flag signal, the first and second return flag signals being routed on the second flag signal line with the control and address buses.

60 A method of transferring data in a memory system having a stub configuration comprising:

generating a first clock signal, a control signal, an address signal and data signals on a data bus at a controller, the data bus, first clock signal, control signal, and address signal being arranged in a stub configuration; and

receiving the first clock signal and the control signal that includes a read or write command at a memory module including memory devices coupled to the controller,

the memory module, in response to the write command, initiating a write operation for writing the data signals from the data bus to the memory devices in synchronization with the first clock signal; and

the memory module, in response to the read command, initiating a read operation for reading data from the memory devices to the data bus in synchronization with the first clock signal and generating a second clock signal in response to the first clock signal, the second clock signal being provided to the controller, the controller receiving the data signals on the data bus in response to the second clock signal during the read operation.

61 The method of claim 60 wherein the memory module comprises multiple memory modules and wherein the multiple memory modules each generate independent second clock signals, the multiple independent second clock signals each being different in phase.

62 The method of claim 60 further comprising generating a first flag signal at the controller, the memory module, in response to the first flag signal, controlling timing of initiation of the write operation or read operation, and if a read operation is commanded, generating a second flag signal in response to the first flag signal, the second flag signal being provided to the controller, the controller receiving the data signals on the data bus in response to the second clock signal and the second flag signal during a read operation.

63 A method of transferring data in a memory system having a stub configuration comprising:

generating a first flag signal, a control signal, an address signal, and data signals on a data bus at a controller, the data bus, first flag signal, control signal, and address signal being arranged in a stub configuration; and

receiving the first flag signal and the control signal that includes a read or write command at a memory module including memory devices coupled to the controller;

the memory module, in response to the write command, initiating a write operation for writing the data signals from the data bus to the memory devices in response to the first flag signal; and

the memory module, in response to the read command, initiating a read operation for reading data from the memory devices to the data bus in response to the first flag signal and generating a second flag signal in response to the first flag signal, the second flag signal being provided to the controller, the controller receiving the data signals on the data bus in response to the second flag signal during the read operation.

64 The method of claim 63 further comprising generating a first clock signal at the controller, the memory module, in response to the first clock signal, initiating the write operation or read operation, and if a read operation is commanded, generating a second clock signal in response to the first clock signal, the second clock signal being provided to the controller, the controller receiving the data signals on the data bus in response to the second clock signal and the second flag signal during a read operation.

65 A method of transferring data in a memory system having a stub configuration comprising:

generating a first clock signal, a control signal, an address signal and data signals on a data bus at a controller, the data bus, first clock signal, control signal, and address signal being arranged in a stub configuration;

generating a second clock signal at a second clock signal generator;

receiving the first clock signal, the second clock signal and the control signal that includes a read or write command at a memory module including memory devices coupled to the controller;

transmitting the first clock signal from the controller to the memory module in a first direction of propagation, and transmitting the second clock signal from the memory module to the controller in a second direction of propagation;

the memory module, in response to the write command, initiating a write operation for writing the data signals from the data bus to the memory devices in synchronization with the first clock signal; and

the memory module, in response to the read command, initiating a read operation for reading data from the memory to the data bus in response to the second clock signal, the controller receiving the data signals on the data bus in response to the second clock signal during the read operation.